Lógica Computacional 2024/2025 - TP2

Grupo 6

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In [ ]:
```
!pip install pysmt
!pysmt-install --z3

from z3 import *
import random
```

Exercício 1

Enunciado

Considere a descrição da cifra A5/1. Pretende-se

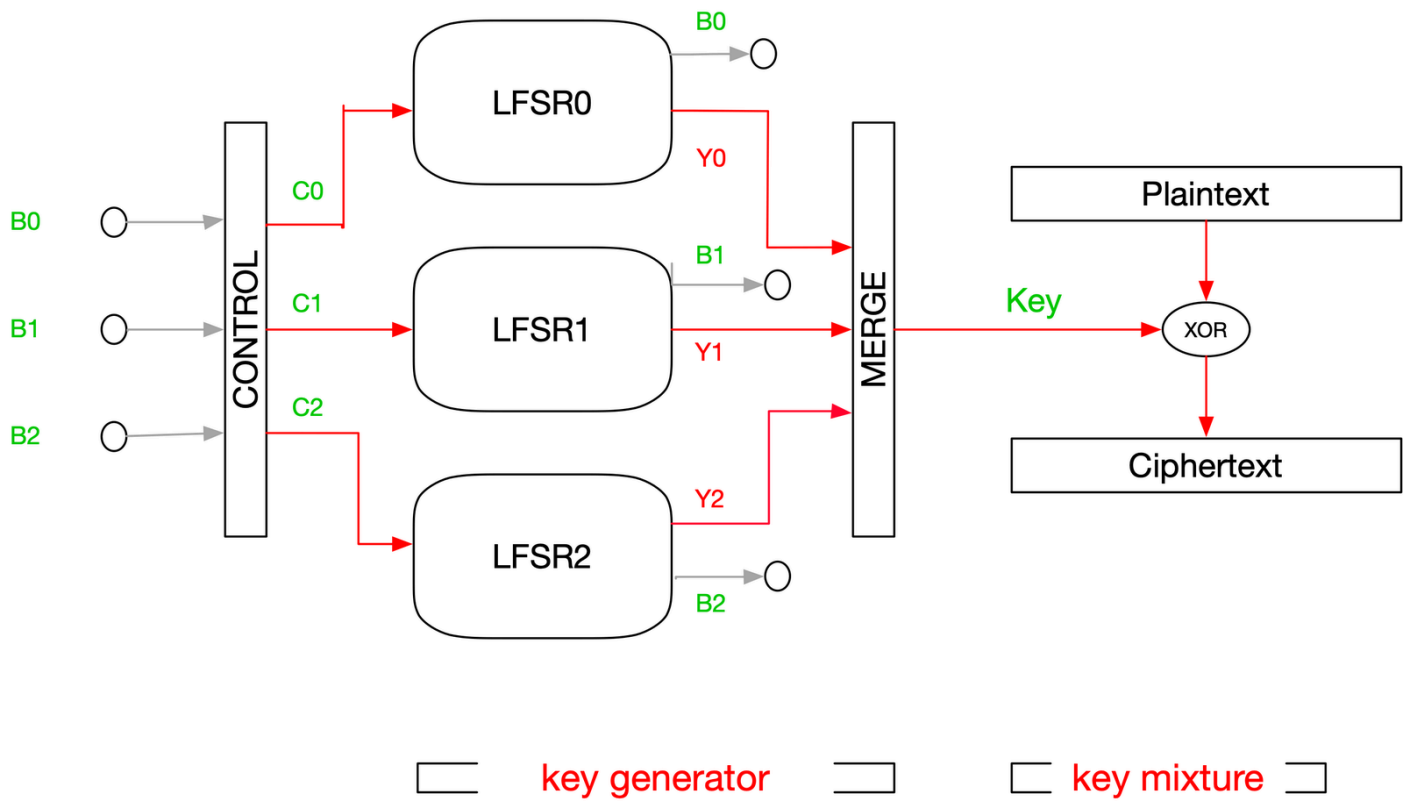
a) Definir e codificar, em Z3 e usando o tipo BitVec para modelar a informação, uma FSM que descreva o gerador de chaves.

b) Considere as seguintes eventuais propriedades de erro:

- ocorrência de um "burst" 0^t (t zeros) que ocorre em 2^t passos ou menos.
- ocorrência de um "burst" de tamanho t que repete um "burst" anterior no mesmo output em 2^(t/2) passos ou menos.

Tente codificar estas propriedades e verificar se são acessíveis a partir de um estado inicial aleatoriamente gerado.

Resolução



Começamos por definir as seguintes funções:

- Função ***declare(i)***, que declara o estado do sistema (os 3 LFSR, a key e a posição do último bit colocado na key) em cada instante i;
- Função ***init(state)***, que gera estados iniciais do sistema com valores aleatórios para cada LFSR;
- Função ***majority (a, b, c)*** que retorna o bit majoritário entre três bits dados;
- Função ***proximo_estado(s)***, que calcula o próximo estado do sistema a partir do estado atual;
- Função ***trans(curr, prox)***, que define a transição entre o estado atual e o próximo estado.

A função *proximo_estado* calcula o *clocking bit* de cada LSFR (no LFSR 0, é o bit de índice 8 e, nos LFSRs 1 e 2, é o bit de índice 10). A partir destes 3 bits, chama a função majority e calcula o *bit majoritário*.

A seguir, a função atualiza cada LSFR. Na cifra A5/1, cada LSFR é deslocado apenas se o seu *bit de controlo* é o *bit majoritário*, bit que calculamos anteriormente. Se o seu *bit de controlo* for diferente, então não é deslocado.

Posteriormente, construímos o novo bit através da operação *merge*. Neste caso, calculamos o *XOR* dos bits mais significativos de cada LSFR.

No final, atualizamos a posição atual no vetor dos *Key Bits* e atualizamos o próprio vetor.

In [ ]:
```python
def declare(i):
    return {
        'LFSR_0': BitVec(f'LFSR_0_{i}', 19),
        'LFSR_1': BitVec(f'LFSR_1_{i}', 22),
        'LFSR_2': BitVec(f'LFSR_2_{i}', 23),
        'keys': BitVec(f'keys_{i}', 64),  # Vetor de 64 bits
        'keys_pos': BitVec(f'keys_pos_{i}', 7)  # Posição atual no vetor (0-63), representada por 7 bits
    }

def init(state):
    z0 = random.getrandbits(19)
    z1 = random.getrandbits(22)
    z2 = random.getrandbits(23)

    return And(
        state['LFSR_0'] == BitVecVal(z0, 19),
        state['LFSR_1'] == BitVecVal(z1, 22),
        state['LFSR_2'] == BitVecVal(z2, 23),
        state['keys'] == BitVecVal(0, 64),  # Inicializado com zero
        state['keys_pos'] == BitVecVal(0, 7)  # Posição inicializada com zero
    )

def majority(a, b, c):
    return (a & b) | (b & c) | (c & a)

def proximo_estado(s):
    c0 = Extract(8, 8, s['LFSR_0'])
    c1 = Extract(10, 10, s['LFSR_1'])
    c2 = Extract(10, 10, s['LFSR_2'])

    maj = majority(c0, c1, c2)

    # Desloca os LFSR e atualiza usando uma função XOR
    updated_LFSR_0 = If(c0 == maj,
                Concat(Extract(17, 0, s['LFSR_0']),
                       Extract(18, 18, s['LFSR_0']) ^ Extract(17, 17, s['LFSR_0']) ^
                       Extract(16, 16, s['LFSR_0']) ^ Extract(13, 13, s['LFSR_0'])),
                s['LFSR_0'])

    updated_LFSR_1 = If(c1 == maj,
                Concat(Extract(20, 0, s['LFSR_1']),
                       Extract(21, 21, s['LFSR_1']) ^ Extract(20, 20, s['LFSR_1'])),
                s['LFSR_1'])

    updated_LFSR_2 = If(c2 == maj,
                Concat(Extract(21, 0, s['LFSR_2']),
                       Extract(22, 22, s['LFSR_2']) ^ Extract(21, 21, s['LFSR_2']) ^
                       Extract(20, 20, s['LFSR_2']) ^ Extract(7, 7, s['LFSR_2'])),
                s['LFSR_2'])

    # XOR dos bits mais significativos
    updated_bit = Extract(18, 18, updated_LFSR_0) ^ Extract(21, 21, updated_LFSR_1) ^ Extract(22, 22, updated_LFSR_2)

    # Atualiza a posição do vetor
    updated_pos = s['keys_pos'] + 1

    # Atualiza o vetor inserindo o novo bit se a posição for menor que 63
    updated_keys = If(ULT(s['keys_pos'], BitVecVal(63, 7)),
                   s['keys'] | (ZeroExt(63, updated_bit) << ZeroExt(57, s['keys_pos'])),
                   s['keys'])

    return {
        'LFSR_0': updated_LFSR_0,
        'LFSR_1': updated_LFSR_1,
        'LFSR_2': updated_LFSR_2,
        'keys': updated_keys,
        'keys_pos': updated_pos
    }

def trans(curr, prox):
    proximo = proximo_estado(curr)
    return And(
        prox['LFSR_0'] == proximo['LFSR_0'],
        prox['LFSR_1'] == proximo['LFSR_1'],
        prox['LFSR_2'] == proximo['LFSR_2'],
        prox['keys'] == proximo['keys'],
        prox['keys_pos'] == proximo['keys_pos']
    )
```

Definimos as propriedades de erro da alínea b) em duas funções.

- A função ***check_burst_zeros(bits, t, pos)*** verifica se há um burst de zeros contínuos de comprimento 't' no output inicializado.
- A função ***check_burst_repetido(bits, t, pos)*** verifica se há um burst de bits repetidos de comprimento 't' no output inicializado.

In [ ]:
```python
def check_burst_zeros(bits, t, pos):
    max_pos = pos.as_long() # Valor máximo da posição
    # Itera de 0 até max_pos - t + 1 (todas as posições possíveis), extrai sequência de t bits e adiciona a lista
    # Resultado de Or sobre a lista verifica se alguma sequência tem t bits zero
    return Or([Extract(i + t - 1, i, bits) == 0 for i in range(max_pos - t + 1)])

def check_burst_repetido(bits, t, pos):
    max_pos = pos.as_long() # Valor máximo da posição
    # Resultado de Or sobre a lista verifica se alguma é repetida
    return Or([And(Extract(i + t - 1, i, bits) == Extract(j + t - 1, j, bits), # Extrai sequência de t bits
                   i != j, # Sequências devem ser diferentes
                   j - i <= 2 ** (t // 2)) # Distância entre as sequências deve ser no máximo 2 ** (t // 2)
               for i in range(max_pos - t + 1) # 0 até max_pos - t + 1 (todas as posições possíveis)
               for j in range(i + 1, min(i + 2 ** (t // 2) + 1, max_pos - t + 1))]) # i + 1 até min(i + 2 ** (t // 2) + 1, max_pos - t + 1)
                                                                                     # (posições que estão a uma distância de no máximo 2 ** (t // 2) de i)
```

A função ***gera_traco(declare, init, trans, k, t)*** começa por declarar, inicializar o sistema e o Solver e definir a evolução do sistema em cada transição. É criada uma lista vazia *detectado*, onde serão colocados todos os estados em que for detectada uma propriedade de erro. Em cada estado, verifica-se as propriedades de erro e, para visualização, é imprimido cada LFSR, o vetor *Key Bits* para cada estado e a ocorrência de propriedade de erro, se for o caso. No final, se tiver sido detectada alguma propriedade de erro, os estados em que ocorreu são listados.

In [ ]:
```
def gera_traco(declare, init, trans, k, t):
    states = [declare(i) for i in range(k + 1)] # Declara o estado do sistema
    solver = Solver() # Inicializa o Solver
    solver.add(init(states[0])) # Inicializa aleatoriamente o sistema

    for i in range(k):
        solver.add(trans(states[i], states[i + 1])) # Define evolução do sistema

    detectado = []
    for i, state in enumerate(states):
        # Verifica se o solver é satisfatório antes de chamar o modelo
        if solver.check() == sat:
            model = solver.model()
            LFSR_0_val = model[state['LFSR_0']].as_long() # as_long converte BitVec para número inteiro
            LFSR_1_val = model[state['LFSR_1']].as_long()
            LFSR_2_val = model[state['LFSR_2']].as_long()
            keys_val = model[state['keys']].as_long()
            pos_val = model[state['keys_pos']].as_long()

            # Imprime
            print(f"\nEstado {i}:")
            print("-" * 40)
            LFSR_0_bin = bin(LFSR_0_val)[2:].zfill(19) # bin converte número inteiro para binário
            LFSR_1_bin = bin(LFSR_1_val)[2:].zfill(22) # remove '0b' , zfill() preenche a string com zeros à esquerda até atingir o comprimento
            LFSR_2_bin = bin(LFSR_2_val)[2:].zfill(23)
            keys_bin = bin(keys_val)[2:].zfill(64)
            print(f"LFSR 0: {LFSR_0_bin}")
            print(f"LFSR 1: {LFSR_1_bin}")
            print(f"LFSR 2: {LFSR_2_bin}")
            print(f"Output ({pos_val} bits preenchidos): {keys_bin}")

            # Verifica as propriedades de erro
            if pos_val > 0:  # Não se verifica o estado inicial
                burst_zeros = check_burst_zeros(state['keys'], t, BitVecVal(pos_val, 7))
                burst_repetido = check_burst_repetido(state['keys'], t, BitVecVal(pos_val, 7))

                if solver.check(burst_zeros) == sat:
                    print("*** Burst de zeros detectado neste estado ***")
                    detectado.append(i)
                if solver.check(burst_repetido) == sat:
                    print("*** Burst repetido detectado neste estado ***")
                    detectado.append(i)
        else:
            print(f"> Erro ao gerar estado {i}.")

    if detectado:
        print(f"\nPropriedades de erro detectadas nos estados: {sorted(set(detectado))}")
    else:
        print(f"\n> Nenhuma propriedade de erro detectada para burst de tamanho {t}.")
```

Por fim, podemos testar o código para o número de iterações e o tamanho de burst que desejarmos. Para que seja possível visualizar os Key Bits todos, o número de iterações deve ser menor que 64.

In [ ]:
```
k = int(input("Forneça um número de iterações: "))
print(f"Calcular com número de iterações = {k}...\n")
t = int(input("Forneça um tamanho de burst: "))
print(f"Calcular com tamanho = {t}...\n")

gera_traco(declare, init, trans, k, t)
```

```
Forneça um número de iterações: 40
Calcular com traço = 40...

Forneça um tamanho de burst: 4
Calcular com tamanho = 4...


Estado 0:
----------------------------------------
LFSR 0: 1110001101011110010
LFSR 1: 1111111110101110010101
LFSR 2: 0110000111010110000110
Output (0 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 1:
----------------------------------------
LFSR 0: 1100011010111100101
LFSR 1: 1111111101011100101010
LFSR 2: 1100001110101100001100
Output (1 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000001

Estado 2:
----------------------------------------
LFSR 0: 1000110101111001011
LFSR 1: 1111111010111001010100
LFSR 2: 1000011101011000011000
Output (2 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000011

Estado 3:
----------------------------------------
LFSR 0: 0001101011110010110
LFSR 1: 1111110101110010101000
LFSR 2: 0000111010110000110001
Output (3 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000111

Estado 4:
----------------------------------------
LFSR 0: 0011010111100101100
LFSR 1: 1111101011100101010000
LFSR 2: 0000111010110000110001
Output (4 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000001111

Estado 5:
----------------------------------------
LFSR 0: 0011010111100101100
LFSR 1: 1111010111001010100000
LFSR 2: 0001110101100001100010
Output (5 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000011111
*** Burst repetido detectado neste estado ***

Estado 6:
----------------------------------------
LFSR 0: 0011010111100101100
LFSR 1: 1110101110010101000000
LFSR 2: 0011101011000011000100
Output (6 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000111111
*** Burst repetido detectado neste estado ***

Estado 7:
----------------------------------------
LFSR 0: 0110101111001011000
LFSR 1: 1101011100101010000000
LFSR 2: 0011101011000011000100
Output (7 bits preenchidos): 0000000000000000000000000000000000000000000000000000000001111111
*** Burst repetido detectado neste estado ***

Estado 8:
----------------------------------------
LFSR 0: 1101011110010110000
LFSR 1: 1010111001010100000000
LFSR 2: 0111010110000011000100
Output (8 bits preenchidos): 0000000000000000000000000000000000000000000000000000000001111111
*** Burst repetido detectado neste estado ***

Estado 9:
----------------------------------------
LFSR 0: 1010111100101100001
LFSR 1: 1010111001010100000000
LFSR 2: 1110101100001100010001
Output (9 bits preenchidos): 0000000000000000000000000000000000000000000000000000000101111111
*** Burst repetido detectado neste estado ***

Estado 10:
----------------------------------------
LFSR 0: 0101111001011000011
LFSR 1: 0101110010101000000001
LFSR 2: 1110101100001100010001
Output (10 bits preenchidos): 0000000000000000000000000000000000000000000000000000001101111111
*** Burst repetido detectado neste estado ***

Estado 11:
----------------------------------------
LFSR 0: 1011110010110000110
LFSR 1: 1011100101010000000011
LFSR 2: 1101011000011000100011
Output (11 bits preenchidos): 0000000000000000000000000000000000000000000000000000011101111111
*** Burst repetido detectado neste estado ***

Estado 12:
----------------------------------------
LFSR 0: 0111100101100001101
LFSR 1: 0111001010100000000111
```

```
LFSR 2: 1010110000110001000110
Output (12 bits preenchidos): 000000000000000000000000000000000000000000000000000111101111111
*** Burst repetido detectado neste estado ***

Estado 13:
----------------------------------------
LFSR 0: 1111001011000011010
LFSR 1: 0111001010100000000111
LFSR 2: 0101100000110001001100
Output (13 bits preenchidos): 0000000000000000000000000000000000000000000000000011111101111111
*** Burst repetido detectado neste estado ***

Estado 14:
----------------------------------------
LFSR 0: 1110010110000110101
LFSR 1: 1110010101000000001111
LFSR 2: 1011000011000100011000
Output (14 bits preenchidos): 0000000000000000000000000000000000000000000000000111111101111111
*** Burst repetido detectado neste estado ***

Estado 15:
----------------------------------------
LFSR 0: 1100101100001101010
LFSR 1: 1100101010000000011110
LFSR 2: 0110000011000100011000 0
Output (15 bits preenchidos): 0000000000000000000000000000000000000000000000000011111101111111
*** Burst repetido detectado neste estado ***

Estado 16:
----------------------------------------
LFSR 0: 1001011000011010100
LFSR 1: 1001010100000000111100
LFSR 2: 1100000110001000110000 0
Output (16 bits preenchidos): 0000000000000000000000000000000000000000000000001011111101111111
*** Burst repetido detectado neste estado ***

Estado 17:
----------------------------------------
LFSR 0: 0010110000110101000
LFSR 1: 0010101000000001111001
LFSR 2: 1100000110001000110000 0
Output (17 bits preenchidos): 0000000000000000000000000000000000000000000000011011111101111111
*** Burst repetido detectado neste estado ***

Estado 18:
----------------------------------------
LFSR 0: 0101100001101010000
LFSR 1: 0010101000000001111001
LFSR 2: 1000001100010011000000
Output (18 bits preenchidos): 0000000000000000000000000000000000000000000000111011111101111111
*** Burst repetido detectado neste estado ***

Estado 19:
----------------------------------------
LFSR 0: 0101100001101010000
LFSR 1: 0101010000000111110010
LFSR 2: 0000011000100011000000
Output (19 bits preenchidos): 0000000000000000000000000000000000000000000000111011111101111111
*** Burst repetido detectado neste estado ***

Estado 20:
----------------------------------------
LFSR 0: 0101100001101010000
LFSR 1: 1010100000000111100101
LFSR 2: 0000110001000110000001
Output (20 bits preenchidos): 0000000000000000000000000000000000000000000000101110111111101111111
*** Burst repetido detectado neste estado ***

Estado 21:
----------------------------------------
LFSR 0: 0101100001101010000
LFSR 1: 0101000000001111001011
LFSR 2: 0001100010001100000010
Output (21 bits preenchidos): 0000000000000000000000000000000000000000000000101110111111101111111
*** Burst repetido detectado neste estado ***

Estado 22:
----------------------------------------
LFSR 0: 1011000011010100001
LFSR 1: 0101000000001111001011
LFSR 2: 0011000100011000000100
Output (22 bits preenchidos): 0000000000000000000000000000000000000000000010101110111111101111111
*** Burst repetido detectado neste estado ***

Estado 23:
----------------------------------------
LFSR 0: 0110000110101000010
LFSR 1: 1010000000011110010111
LFSR 2: 0011000100011000000100
Output (23 bits preenchidos): 0000000000000000000000000000000000000000000110101110111111101111111
*** Burst repetido detectado neste estado ***

Estado 24:
----------------------------------------
LFSR 0: 1100001101010000100
LFSR 1: 0100000000111100101111
LFSR 2: 0110001000110000001001
Output (24 bits preenchidos): 0000000000000000000000000000000000000000000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 25:
----------------------------------------
```

```
LFSR 0: 1000011010100001000
LFSR 1: 0100000000111100101111
LFSR 2: 1100010001100000010010
Output (25 bits preenchidos): 0000000000000000000000000000000000000000011101011101111111101111111
*** Burst repetido detectado neste estado ***

Estado 26:
----------------------------------------
LFSR 0: 0000110101000010000
LFSR 1: 1000000001111001011111
LFSR 2: 1100010001100000010010
Output (26 bits preenchidos): 0000000000000000000000000000000000000000011101011101111111101111111
*** Burst repetido detectado neste estado ***

Estado 27:
----------------------------------------
LFSR 0: 0001101010000100001
LFSR 1: 1000000001111001011111
LFSR 2: 1000100011000000100100
Output (27 bits preenchidos): 0000000000000000000000000000000000000000011101011101111111101111111
*** Burst repetido detectado neste estado ***

Estado 28:
----------------------------------------
LFSR 0: 0011010100001000010
LFSR 1: 1000000001111001011111
LFSR 2: 0001000110000001001001
Output (28 bits preenchidos): 0000000000000000000000000000000000000100011101011101111111101111111
*** Burst repetido detectado neste estado ***

Estado 29:
----------------------------------------
LFSR 0: 0110101000010000100
LFSR 1: 1000000001111001011111
LFSR 2: 0010001100000010010010
Output (29 bits preenchidos): 0000000000000000000000000000000000011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 30:
----------------------------------------
LFSR 0: 1101010000100001000
LFSR 1: 1000000001111001011111
LFSR 2: 0100011000000100100100
Output (30 bits preenchidos): 0000000000000000000000000000000000011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 31:
----------------------------------------
LFSR 0: 1010100001000010001
LFSR 1: 0000000011110010111111
LFSR 2: 0100011000000100100100
Output (31 bits preenchidos): 0000000000000000000000000000000001011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 32:
----------------------------------------
LFSR 0: 0101000010000100010
LFSR 1: 0000000011110010111111
LFSR 2: 1000110000001001001001
Output (32 bits preenchidos): 0000000000000000000000000000000011011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 33:
----------------------------------------
LFSR 0: 1010000100001000101
LFSR 1: 0000000011110010111111
LFSR 2: 0001100000010010010011
Output (33 bits preenchidos): 0000000000000000000000000000000111011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 34:
----------------------------------------
LFSR 0: 1010000100001000101
LFSR 1: 0000000111100101111110
LFSR 2: 0011000000100100100111
Output (34 bits preenchidos): 0000000000000000000000000000001111011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 35:
----------------------------------------
LFSR 0: 0100001000010001010
LFSR 1: 0000001111001011111100
LFSR 2: 0110000000100100100111
Output (35 bits preenchidos): 0000000000000000000000000000001111011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 36:
----------------------------------------
LFSR 0: 1000010000100010101
LFSR 1: 0000011110010111111000
LFSR 2: 1100000001001001011110
Output (36 bits preenchidos): 0000000000000000000000000000001111011000111010111011111101111111
*** Burst repetido detectado neste estado ***

Estado 37:
----------------------------------------
LFSR 0: 0000100001000101010
LFSR 1: 0000111100101111110000
LFSR 2: 1000000010010010011110 1
Output (37 bits preenchidos): 0000000000000000000000000001001111011000111010111011111101111111
*** Burst repetido detectado neste estado ***
```

```
Estado 38:
----------------------------------------
LFSR 0: 0001000010001010100
LFSR 1: 0001111001011111100000
LFSR 2: 0000000100100100111011
Output (38 bits preenchidos): 00000000000000000000000000100111101100011101011101111101111111
*** Burst repetido detectado neste estado ***

Estado 39:
----------------------------------------
LFSR 0: 0010000100010101000
LFSR 1: 0001111001011111100000
LFSR 2: 0000001001001001111011 0
Output (39 bits preenchidos): 00000000000000000000000000100111101100011101011101111101111111
*** Burst repetido detectado neste estado ***

Estado 40:
----------------------------------------
LFSR 0: 0010000100010101000
LFSR 1: 0011110010111111000000
LFSR 2: 0000010010010011101101
Output (40 bits preenchidos): 00000000000000000000000000100111101100011101011101111101111111
*** Burst repetido detectado neste estado ***

Propriedades de erro detectadas nos estados: [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30,
31, 32, 33, 34, 35, 36, 37, 38, 39, 40]
```

Interpretação dos resultados

Diferentes testes apoiam a nossa interpretação das propriedades de erro. Experimente os seguintes testes:

In [ ]:
```python
print("-" * 100)
print("\nPara k = 30 e t = 4:")
gera_traco(declare, init, trans, 30, 4)

print("-" * 100)
print("\nPara k = 30 e t = 20:")
gera_traco(declare, init, trans, 30, 20)

print("-" * 100)
print("\nPara k = 64 e t = 4:")
gera_traco(declare, init, trans, 64, 4)

print("-" * 100)
print("\nPara k = 64 e t = 20:")
gera_traco(declare, init, trans, 64, 20)
```

```
----------------------------------------------------------------------------------------------------

Para k = 30 e t = 4:

Estado 0:
----------------------------------------
LFSR 0: 1011111110011011011
LFSR 1: 1000101101101000111010
LFSR 2: 1000100011001001010100 1
Output (0 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000

Estado 1:
----------------------------------------
LFSR 0: 0111111100110110111
LFSR 1: 0001011011010001110101
LFSR 2: 1000100011001001010100 1
Output (1 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000001

Estado 2:
----------------------------------------
LFSR 0: 1111111001101101111
LFSR 1: 0010110110100011101010
LFSR 2: 0001000110010010101001 0
Output (2 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000011

Estado 3:
----------------------------------------
LFSR 0: 1111111001101101111
LFSR 1: 0101101101000111010100
LFSR 2: 0010001100100101010010 0
Output (3 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000111

Estado 4:
----------------------------------------
LFSR 0: 1111111001101101111
LFSR 1: 1011011010001110101001
LFSR 2: 0100011001001010100100 0
Output (4 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000111

Estado 5:
----------------------------------------
LFSR 0: 1111110011011011110
LFSR 1: 1011011010001110101001
LFSR 2: 1000110010010101001000 1
Output (5 bits preenchidos): 000000000000000000000000000000000000000000000000000000000010111

Estado 6:
----------------------------------------
LFSR 0: 1111100110110111100
LFSR 1: 0110110100011101010011
LFSR 2: 0001100100101010010001 0
Output (6 bits preenchidos): 000000000000000000000000000000000000000000000000000000000110111

Estado 7:
----------------------------------------
LFSR 0: 1111001101101111001
LFSR 1: 1101101000111010100111
LFSR 2: 0011001001010100100010 0
Output (7 bits preenchidos): 000000000000000000000000000000000000000000000000000000000110111

Estado 8:
----------------------------------------
LFSR 0: 1110011011011110011
LFSR 1: 1011010001110101001110
LFSR 2: 0011001001010100100010 0
Output (8 bits preenchidos): 000000000000000000000000000000000000000000000000000000000110111

Estado 9:
----------------------------------------
LFSR 0: 1100110110111100110
LFSR 1: 1011010001110101001110
LFSR 2: 0110010010101001000100 1
Output (9 bits preenchidos): 000000000000000000000000000000000000000000000000000000000110111

Estado 10:
----------------------------------------
LFSR 0: 1001101101111001101
LFSR 1: 0110100011101010011101
LFSR 2: 1100100101010010001001 1
Output (10 bits preenchidos): 000000000000000000000000000000000000000000000000000000000110111
*** Burst de zeros detectado neste estado ***

Estado 11:
----------------------------------------
LFSR 0: 1001101101111001101
LFSR 1: 1101000111010100111011
LFSR 2: 1001001010100100010011 0
Output (11 bits preenchidos): 000000000000000000000000000000000000000000000000000010000110111
*** Burst de zeros detectado neste estado ***

Estado 12:
----------------------------------------
LFSR 0: 0011011011110011011
LFSR 1: 1010001110101001110110
LFSR 2: 1001001010100100010011 0
Output (12 bits preenchidos): 000000000000000000000000000000000000000000000000000010000110111
*** Burst de zeros detectado neste estado ***

Estado 13:
----------------------------------------
LFSR 0: 0011011011110011011
LFSR 1: 0100011101010011101101
```

```
LFSR 2: 0010010101001000100110 1
Output (13 bits preenchidos): 0000000000000000000000000000000000000000000000000000010000110111
*** Burst de zeros detectado neste estado ***

Estado 14:
----------------------------------------
LFSR 0: 0110110111100110110
LFSR 1: 1000111010100111011011
LFSR 2: 0100101010010001001101 1
Output (14 bits preenchidos): 0000000000000000000000000000000000000000000000000100100000110111
*** Burst de zeros detectado neste estado ***

Estado 15:
----------------------------------------
LFSR 0: 0110110111100110110
LFSR 1: 0001110101001110110111
LFSR 2: 1001010100100010011011 0
Output (15 bits preenchidos): 0000000000000000000000000000000000000000000000001100100000110111
*** Burst de zeros detectado neste estado ***

Estado 16:
----------------------------------------
LFSR 0: 0110110111100110110
LFSR 1: 0011101010011101101110
LFSR 2: 0010101001000100110110 1
Output (16 bits preenchidos): 0000000000000000000000000000000000000000000000011001000011011 1
*** Burst de zeros detectado neste estado ***

Estado 17:
----------------------------------------
LFSR 0: 1101101111001101101
LFSR 1: 0111010100111011011100
LFSR 2: 0010101001000100110110 1
Output (17 bits preenchidos): 0000000000000000000000000000000000000000000000101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 18:
----------------------------------------
LFSR 0: 1011011110011011010
LFSR 1: 0111010100111011011100
LFSR 2: 0101010010001001101101 1
Output (18 bits preenchidos): 0000000000000000000000000000000000000000000001101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 19:
----------------------------------------
LFSR 0: 1011011110011011010
LFSR 1: 1110101001110110111001
LFSR 2: 1010100100010011011011 0
Output (19 bits preenchidos): 0000000000000000000000000000000000000000000011101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 20:
----------------------------------------
LFSR 0: 0110111100110110101
LFSR 1: 1110101001110110111001
LFSR 2: 0101001000100110110110 1
Output (20 bits preenchidos): 0000000000000000000000000000000000000000000011101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 21:
----------------------------------------
LFSR 0: 1101111001101101011
LFSR 1: 1101010011101101110010
LFSR 2: 0101001000100110110110 1
Output (21 bits preenchidos): 0000000000000000000000000000000000000000000011101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 22:
----------------------------------------
LFSR 0: 1101111001101101011
LFSR 1: 1010100111011011100100
LFSR 2: 1010010001001101101101 1
Output (22 bits preenchidos): 0000000000000000000000000000000000000000000010111101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 23:
----------------------------------------
LFSR 0: 1011110011011010111
LFSR 1: 0101001110110111001001
LFSR 2: 0100100010011011011011 1
Output (23 bits preenchidos): 0000000000000000000000000000000000000000000110111101100100000110111
*** Burst de zeros detectado neste estado ***

Estado 24:
----------------------------------------
LFSR 0: 1011110011011010111
LFSR 1: 1010011101101110010011
LFSR 2: 1001000100110110110111 0
Output (24 bits preenchidos): 0000000000000000000000000000000000000000000001101111011001000011011 1
*** Burst de zeros detectado neste estado ***

Estado 25:
----------------------------------------
LFSR 0: 0111100110110101111
LFSR 1: 0100111011011100100111
LFSR 2: 0010001001101101101110 1
Output (25 bits preenchidos): 0000000000000000000000000000000000000000000001101111011001000011011 1
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 26:
```

```
----------------------------------------
LFSR 0: 1111001101101011110
LFSR 1: 1001110110111001001111
LFSR 2: 0100010011011011011110
Output (26 bits preenchidos): 00000000000000000000000000000000000000000111011110110010000110111
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 27:
----------------------------------------
LFSR 0: 1110011011010111101
LFSR 1: 0011101101110010011111
LFSR 2: 1000100110110110110100
Output (27 bits preenchidos): 00000000000000000000000000000000000000000111011110110010000110111
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 28:
----------------------------------------
LFSR 0: 1100110110101111010
LFSR 1: 0011101101110010011111
LFSR 2: 0001001101101101101001
Output (28 bits preenchidos): 00000000000000000000000000000000000000100011101111011100100000110111
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 29:
----------------------------------------
LFSR 0: 1001101101011110101
LFSR 1: 0111011011100100111110
LFSR 2: 0010011011011011101001 1
Output (29 bits preenchidos): 00000000000000000000000000000000000000110001110111101100100000110111
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 30:
----------------------------------------
LFSR 0: 0011011010111101011
LFSR 1: 1110110111001001111101
LFSR 2: 0010011011011011101001 1
Output (30 bits preenchidos): 00000000000000000000000000000000000000111000111011110110010000110111
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Propriedades de erro detectadas nos estados: [10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30]
----------------------------------------------------------------------------------------------------

Para k = 30 e t = 20:

Estado 0:
----------------------------------------
LFSR 0: 1101010011101111101
LFSR 1: 1011011011100000001110
LFSR 2: 1000001100111011101 0000
Output (0 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000000

Estado 1:
----------------------------------------
LFSR 0: 1010100111011111011
LFSR 1: 1011011011100000001110
LFSR 2: 0000011001110111010000 0
Output (1 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000000

Estado 2:
----------------------------------------
LFSR 0: 0101001110111110110
LFSR 1: 0110110111000000011101
LFSR 2: 0000110011101110100000 1
Output (2 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000000

Estado 3:
----------------------------------------
LFSR 0: 1010011101111101101
LFSR 1: 0110110111000000011101
LFSR 2: 0001100111011101000001 0
Output (3 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000100

Estado 4:
----------------------------------------
LFSR 0: 0100111011111011011
LFSR 1: 0110110111000000011101
LFSR 2: 0011001110111010000010 1
Output (4 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000000100

Estado 5:
----------------------------------------
LFSR 0: 1001110111110110110
LFSR 1: 0110110111000000011101
LFSR 2: 0110011101110100000101 1
Output (5 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000010100

Estado 6:
----------------------------------------
LFSR 0: 1001110111110110110
LFSR 1: 1101101110000000111011
LFSR 2: 1100111011101000001011 0
Output (6 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000110100

Estado 7:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 1101101110000000111011
```

```
LFSR 2: 1001110111010000010110 0
Output (7 bits preenchidos): 000000000000000000000000000000000000000000000000000000000000110100

Estado 8:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 1011011100000001110110
LFSR 2: 0011101110100000101100 1
Output (8 bits preenchidos): 000000000000000000000000000000000000000000000000000000000010110100

Estado 9:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 0110111000000011101101
LFSR 2: 0111011101000001011001 1
Output (9 bits preenchidos): 000000000000000000000000000000000000000000000000000000000010110100

Estado 10:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 1101110000000111011011
LFSR 2: 1110111010000010110011 1
Output (10 bits preenchidos): 000000000000000000000000000000000000000000000000000000000010110100

Estado 11:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 1011100000001110110110
LFSR 2: 1101110100000101100111 1
Output (11 bits preenchidos): 000000000000000000000000000000000000000000000000000000000010110100

Estado 12:
----------------------------------------
LFSR 0: 0011101111101101100
LFSR 1: 0111000000011101101101
LFSR 2: 1011101000001011001111 1
Output (12 bits preenchidos): 000000000000000000000000000000000000000000000000000100010110100

Estado 13:
----------------------------------------
LFSR 0: 0111011111011011001
LFSR 1: 1110000000111011011011
LFSR 2: 0111010000010110011111 1
Output (13 bits preenchidos): 000000000000000000000000000000000000000000000000001100010110100

Estado 14:
----------------------------------------
LFSR 0: 1110111110110110011
LFSR 1: 1110000000111011011011
LFSR 2: 1110100000101100111111 0
Output (14 bits preenchidos): 000000000000000000000000000000000000000000000000011100010110100

Estado 15:
----------------------------------------
LFSR 0: 1101111101101100110
LFSR 1: 1100000001110110110110
LFSR 2: 1101000001011001111110 1
Output (15 bits preenchidos): 000000000000000000000000000000000000000000000000111100010110100

Estado 16:
----------------------------------------
LFSR 0: 1011111011011001101
LFSR 1: 1000000011101101101100
LFSR 2: 1010000010110011111101 1
Output (16 bits preenchidos): 000000000000000000000000000000000000000000000001111100010110100

Estado 17:
----------------------------------------
LFSR 0: 0111110110110011011
LFSR 1: 0000000111011011011001
LFSR 2: 0100000101100111111011 1
Output (17 bits preenchidos): 000000000000000000000000000000000000000000000011111100010110100

Estado 18:
----------------------------------------
LFSR 0: 1111101101100110111
LFSR 1: 0000001110110110110010
LFSR 2: 0100000101100111111011 1
Output (18 bits preenchidos): 000000000000000000000000000000000000000000000101111100010110100

Estado 19:
----------------------------------------
LFSR 0: 1111011011001101111
LFSR 1: 0000011101101101100100
LFSR 2: 0100000101100111111011 1
Output (19 bits preenchidos): 000000000000000000000000000000000000000000001101111100010110100

Estado 20:
----------------------------------------
LFSR 0: 1110110110011011110
LFSR 1: 0000111011011011001000
LFSR 2: 1000001011001111110111 0
Output (20 bits preenchidos): 000000000000000000000000000000000000000000011011111100010110100

Estado 21:
----------------------------------------
LFSR 0: 1110110110011011110
LFSR 1: 0001110110110110010000
LFSR 2: 0000010110011111101110 0
Output (21 bits preenchidos): 000000000000000000000000000000000000000000101101111100010110100

Estado 22:
```

```
----------------------------------------
LFSR 0: 1110110110011011110
LFSR 1: 0011101101101100100000
LFSR 2: 0000101100111110111001
Output (22 bits preenchidos): 0000000000000000000000000000000000000000000011011011111100010110100

Estado 23:
----------------------------------------
LFSR 0: 1101101100110111100
LFSR 1: 0111011011011001000000
LFSR 2: 0000101100111110111001
Output (23 bits preenchidos): 0000000000000000000000000000000000000000000111011011111100010110100

Estado 24:
----------------------------------------
LFSR 0: 1011011001101111000
LFSR 1: 1110110110110010000001
LFSR 2: 0001011001111110111001 1
Output (24 bits preenchidos): 0000000000000000000000000000000000000000001110110111111000101101 00

Estado 25:
----------------------------------------
LFSR 0: 0110110011011110001
LFSR 1: 1101101101100100000010
LFSR 2: 0010110011111101110011 0
Output (25 bits preenchidos): 0000000000000000000000000000000000000000010111011011111000101101 00

Estado 26:
----------------------------------------
LFSR 0: 1101100110111100011
LFSR 1: 1011011011001000000100
LFSR 2: 0010110011111101110011 0
Output (26 bits preenchidos): 0000000000000000000000000000000000000000101110110111111000101101 00

Estado 27:
----------------------------------------
LFSR 0: 1011001101111000110
LFSR 1: 1011011011001000000100
LFSR 2: 0101100111110111001100
Output (27 bits preenchidos): 0000000000000000000000000000000000000000101110110111111000101101 00

Estado 28:
----------------------------------------
LFSR 0: 0110011011110001100
LFSR 1: 1011011011001000000100
LFSR 2: 1011001111101110011000
Output (28 bits preenchidos): 0000000000000000000000000000000000000000101110110111111000101101 00

Estado 29:
----------------------------------------
LFSR 0: 0110011011110001100
LFSR 1: 0110110110010000001001
LFSR 2: 0110011111101110011000 1
Output (29 bits preenchidos): 0000000000000000000000000000000000000000101110110111111000101101 00

Estado 30:
----------------------------------------
LFSR 0: 1100110111100011001
LFSR 1: 1101101100100000010011
LFSR 2: 1100111111011100110001 0
Output (30 bits preenchidos): 0000000000000000000000000000000000000100001011101101111100010110 100

> Nenhuma propriedade de erro detectada para burst de tamanho 20.
--------------------------------------------------------------------------------------------------

Para k = 64 e t = 4:

Estado 0:
----------------------------------------
LFSR 0: 1000110100001111010
LFSR 1: 0010101100110010011110
LFSR 2: 1001010100010110110010 1
Output (0 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 1:
----------------------------------------
LFSR 0: 0001101000011110100
LFSR 1: 0010101100110010011110
LFSR 2: 0010101000101101100101 1
Output (1 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 2:
----------------------------------------
LFSR 0: 0001101000011110100
LFSR 1: 0101011001100100111100
LFSR 2: 0101010001011011001011 0
Output (2 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 3:
----------------------------------------
LFSR 0: 0011010000111101000
LFSR 1: 1010110011001001111001
LFSR 2: 0101010001011011001011 0
Output (3 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100

Estado 4:
----------------------------------------
LFSR 0: 0110100001111010000
LFSR 1: 1010110011001001111001
LFSR 2: 1010100010110110010110 0
Output (4 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100
```

```
Estado 5:
----------------------------------------
LFSR 0: 0110100001111010000
LFSR 1: 0101100110010011110011
LFSR 2: 0101000101101100101 1000
Output (5 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100

Estado 6:
----------------------------------------
LFSR 0: 1101000011110100000
LFSR 1: 1011001100100111100111
LFSR 2: 1010001011011001011 0001
Output (6 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000100100

Estado 7:
----------------------------------------
LFSR 0: 1010000111101000000
LFSR 1: 1011001100100111100111
LFSR 2: 0100010110110010110 0011
Output (7 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000100100
*** Burst repetido detectado neste estado ***

Estado 8:
----------------------------------------
LFSR 0: 1010000111101000000
LFSR 1: 0110011001001111001111
LFSR 2: 1000101101100101100 0111
Output (8 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000100100
*** Burst repetido detectado neste estado ***

Estado 9:
----------------------------------------
LFSR 0: 1010000111101000000
LFSR 1: 1100110010011110011111
LFSR 2: 0001011011001011000 1110
Output (9 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000100100
*** Burst repetido detectado neste estado ***

Estado 10:
----------------------------------------
LFSR 0: 0100000111010000000
LFSR 1: 1001100100111100111110
LFSR 2: 0010110110010110001 1101
Output (10 bits preenchidos): 0000000000000000000000000000000000000000000000000000001000100100
*** Burst repetido detectado neste estado ***

Estado 11:
----------------------------------------
LFSR 0: 1000011110100000001
LFSR 1: 1001100100111100111110
LFSR 2: 0101101100101100011 1011
Output (11 bits preenchidos): 0000000000000000000000000000000000000000000000000000001000100100
*** Burst repetido detectado neste estado ***

Estado 12:
----------------------------------------
LFSR 0: 0000111101000000010
LFSR 1: 0011001001111001111101
LFSR 2: 1011011001011000111 0111
Output (12 bits preenchidos): 0000000000000000000000000000000000000000000000000000101000100100
*** Burst repetido detectado neste estado ***

Estado 13:
----------------------------------------
LFSR 0: 0000111101000000010
LFSR 1: 0110010011110011111010
LFSR 2: 0110110010110001110 1110
Output (13 bits preenchidos): 0000000000000000000000000000000000000000000000000000101000100100
*** Burst repetido detectado neste estado ***

Estado 14:
----------------------------------------
LFSR 0: 0001111010000000101
LFSR 1: 0110010011110011111010
LFSR 2: 1101100101100011101 1101
Output (14 bits preenchidos): 0000000000000000000000000000000000000000000000000010101000100100
*** Burst repetido detectado neste estado ***

Estado 15:
----------------------------------------
LFSR 0: 0011110100000001011
LFSR 1: 0110010011110011111010
LFSR 2: 1011001011000111011 1011
Output (15 bits preenchidos): 0000000000000000000000000000000000000000000000000110101000100100
*** Burst repetido detectado neste estado ***

Estado 16:
----------------------------------------
LFSR 0: 0111101000000010110
LFSR 1: 0110010011110011111010
LFSR 2: 0110010110001110111 0111
Output (16 bits preenchidos): 0000000000000000000000000000000000000000000000000110101000100100
*** Burst repetido detectado neste estado ***

Estado 17:
----------------------------------------
LFSR 0: 0111101000000010110
LFSR 1: 1100100111100111110101
LFSR 2: 1100101100011101110 1110
Output (17 bits preenchidos): 0000000000000000000000000000000000000000000000000110101000100100
*** Burst repetido detectado neste estado ***
```

```
Estado 18:
----------------------------------------
LFSR 0: 1111010000000101100
LFSR 1: 1001001111001111101010
LFSR 2: 1100101100011101101110
Output (18 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst repetido detectado neste estado ***

Estado 19:
----------------------------------------
LFSR 0: 1110100000001011000
LFSR 1: 0010011110011111010101
LFSR 2: 1100101100011101101110
Output (19 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst repetido detectado neste estado ***

Estado 20:
----------------------------------------
LFSR 0: 1110100000001011000
LFSR 1: 0100111100111110101010
LFSR 2: 1001011000110111011101
Output (20 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst repetido detectado neste estado ***

Estado 21:
----------------------------------------
LFSR 0: 1110100000001011000
LFSR 1: 1001111001111101010101
LFSR 2: 0010110001110111011010
Output (21 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst repetido detectado neste estado ***

Estado 22:
----------------------------------------
LFSR 0: 1101000000010110001
LFSR 1: 1001111001111101010101
LFSR 2: 0101100011101101110100
Output (22 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 23:
----------------------------------------
LFSR 0: 1101000000010110001
LFSR 1: 0011110011111010101011
LFSR 2: 1011000111011011101001
Output (23 bits preenchidos): 000000000000000000000000000000000000000000000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 24:
----------------------------------------
LFSR 0: 1101000000010110001
LFSR 1: 0111100111110101010110
LFSR 2: 0110001110111011010011
Output (24 bits preenchidos): 000000000000000000000000000000000000000100001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 25:
----------------------------------------
LFSR 0: 1101000000010110001
LFSR 1: 1111001111101010101101
LFSR 2: 1100011101111011001 11
Output (25 bits preenchidos): 000000000000000000000000000000000000000110000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 26:
----------------------------------------
LFSR 0: 1010000000101100010
LFSR 1: 1110011111010101011010
LFSR 2: 1000111011101101001111
Output (26 bits preenchidos): 000000000000000000000000000000000000000111000010011010100010 0100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 27:
----------------------------------------
LFSR 0: 0100000001011000100
LFSR 1: 1100111110101010110100
LFSR 2: 0001110111011010011111
Output (27 bits preenchidos): 000000000000000000000000000000000000000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 28:
----------------------------------------
LFSR 0: 1000000010110001001
LFSR 1: 1001111101010101101000
LFSR 2: 0001110111011010011111
Output (28 bits preenchidos): 000000000000000000000000000000000000000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 29:
----------------------------------------
LFSR 0: 0000000101100010011
LFSR 1: 0011110101010110100 01
LFSR 2: 0011101110111010011111
Output (29 bits preenchidos): 000000000000000000000000000000000000000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
```

```
*** Burst repetido detectado neste estado ***

Estado 30:
----------------------------------------
LFSR 0: 0000001011000100110
LFSR 1: 0011111010101011010001
LFSR 2: 0111011101110100111111
Output (30 bits preenchidos): 000000000000000000000000000000000000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 31:
----------------------------------------
LFSR 0: 0000010110001001100
LFSR 1: 0111110101010110100010
LFSR 2: 1110111101110100111111110
Output (31 bits preenchidos): 0000000000000000000000000000000010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 32:
----------------------------------------
LFSR 0: 0000010110001001100
LFSR 1: 1111101010101101000101
LFSR 2: 1101110111010011111100
Output (32 bits preenchidos): 0000000000000000000000000000000010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 33:
----------------------------------------
LFSR 0: 0000101100010011001
LFSR 1: 1111010101011010001010
LFSR 2: 1011101110100111111001
Output (33 bits preenchidos): 0000000000000000000000000000000010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 34:
----------------------------------------
LFSR 0: 0001011000100110010
LFSR 1: 1111010101011010001010
LFSR 2: 0111011101001111110011
Output (34 bits preenchidos): 0000000000000000000000000000000100100011110000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 35:
----------------------------------------
LFSR 0: 0010110001001100101
LFSR 1: 1110101010110100010100
LFSR 2: 1110111010011111100111
Output (35 bits preenchidos): 0000000000000000000000000000000100100011110000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 36:
----------------------------------------
LFSR 0: 0010110001001100101
LFSR 1: 1101010101101000101000
LFSR 2: 1101110100111111001110
Output (36 bits preenchidos): 0000000000000000000000000000000100100011110000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 37:
----------------------------------------
LFSR 0: 0101100010011001010
LFSR 1: 1010101011010001010000
LFSR 2: 1101110100111111001110
Output (37 bits preenchidos): 0000000000000000000000000000000100100011110000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 38:
----------------------------------------
LFSR 0: 0101100010011001010
LFSR 1: 0101010110100010100001
LFSR 2: 1011101001111110011101
Output (38 bits preenchidos): 0000000000000000000000000100100100011110000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 39:
----------------------------------------
LFSR 0: 1011000100110010101
LFSR 1: 1010101101000101000011
LFSR 2: 1011101001111110011101
Output (39 bits preenchidos): 0000000000000000000000001100010010001111000010011010100010 0100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 40:
----------------------------------------
LFSR 0: 0110001001100101010
LFSR 1: 1010101101000101000011
LFSR 2: 0111010011111100111011
Output (40 bits preenchidos): 0000000000000000000000011100010010001111000010011010100010 0100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 41:
```

```
----------------------------------------
LFSR 0: 1100010011001010100
LFSR 1: 1010101101000101000011
LFSR 2: 1110100111111001110110
Output (41 bits preenchidos): 00000000000000000000000111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 42:
----------------------------------------
LFSR 0: 1000100110010101001
LFSR 1: 0101011010001010000111
LFSR 2: 1110100111111001110110
Output (42 bits preenchidos): 00000000000000000000000111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 43:
----------------------------------------
LFSR 0: 0001001100101010011
LFSR 1: 1010110100010100001111
LFSR 2: 1110100111111001110110
Output (43 bits preenchidos): 00000000000000000000000111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 44:
----------------------------------------
LFSR 0: 0010011001010100110
LFSR 1: 0101101000101000011111
LFSR 2: 1101001111110011101101
Output (44 bits preenchidos): 00000000000000000000010011110001001000111100000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 45:
----------------------------------------
LFSR 0: 0100110010101001100
LFSR 1: 1011010001010000111111
LFSR 2: 1101001111110011101101
Output (45 bits preenchidos): 00000000000000000000010011110001001000111100000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 46:
----------------------------------------
LFSR 0: 1001100101010011000
LFSR 1: 0110100010100001111111
LFSR 2: 1010011111100111011011
Output (46 bits preenchidos): 00000000000000000000010011110001001000111100000100110101000100 100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 47:
----------------------------------------
LFSR 0: 0011001010100110001
LFSR 1: 1101000101000111111111
LFSR 2: 0100111111001110110111
Output (47 bits preenchidos): 00000000000000000100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 48:
----------------------------------------
LFSR 0: 0011001010100110001
LFSR 1: 1010001010000111111110
LFSR 2: 1001111111001110110111
Output (48 bits preenchidos): 00000000000000000100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 49:
----------------------------------------
LFSR 0: 0110010101001100011
LFSR 1: 1010001010000111111110
LFSR 2: 0011111110011101101110 1
Output (49 bits preenchidos): 00000000000000010100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 50:
----------------------------------------
LFSR 0: 1100101010011000111
LFSR 1: 0100010100001111111101
LFSR 2: 0011111110011101101110 1
Output (50 bits preenchidos): 00000000000000110100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 51:
----------------------------------------
LFSR 0: 1001010100110001110
LFSR 1: 1000101000011111111011
LFSR 2: 0011111110011101101110 1
Output (51 bits preenchidos): 00000000000000110100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 52:
----------------------------------------
LFSR 0: 0010101001100011100
LFSR 1: 0001010000111111110111
```

```
LFSR 2: 0111111100111011011101 0
Output (52 bits preenchidos): 0000000000000011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 53:
----------------------------------------
LFSR 0: 0101010011000111001
LFSR 1: 0010100001111111101110
LFSR 2: 1111111001110110111010 1
Output (53 bits preenchidos): 00000000000100110100100111100010010001111000001001101010001001 00
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 54:
----------------------------------------
LFSR 0: 1010100110001110010
LFSR 1: 0010100001111111101110
LFSR 2: 1111110011101101101011
Output (54 bits preenchidos): 000000000001001101001001111000100100011110000010011010100010010 0
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 55:
----------------------------------------
LFSR 0: 1010100110001110010
LFSR 1: 0101000011111111011100
LFSR 2: 1111100111011011101110
Output (55 bits preenchidos): 0000000000010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 56:
----------------------------------------
LFSR 0: 1010100110001110010
LFSR 1: 1010000111111110111001
LFSR 2: 1111001110110111010110 0
Output (56 bits preenchidos): 0000000010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 57:
----------------------------------------
LFSR 0: 0101001100011100100
LFSR 1: 1010000111111110111001
LFSR 2: 1110011101101110101 1000
Output (57 bits preenchidos): 0000000010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 58:
----------------------------------------
LFSR 0: 0101001100011100100
LFSR 1: 0100001111111101110011
LFSR 2: 1100111011011101011 0001
Output (58 bits preenchidos): 0000001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 59:
----------------------------------------
LFSR 0: 0101001100011100100
LFSR 1: 1000011111111011100111
LFSR 2: 1001110110111010110 0011
Output (59 bits preenchidos): 0000001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 60:
----------------------------------------
LFSR 0: 0101001100011100100
LFSR 1: 0000111111110111001111
LFSR 2: 0011101101110101100011 1
Output (60 bits preenchidos): 0000001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 61:
----------------------------------------
LFSR 0: 1010011000111001001
LFSR 1: 0000111111110111001111
LFSR 2: 0111011011101011000111 0
Output (61 bits preenchidos): 0001001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 62:
----------------------------------------
LFSR 0: 0100110001110010011
LFSR 1: 0001111111101110011110
LFSR 2: 1110110111010110001110 1
Output (62 bits preenchidos): 0011001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Estado 63:
----------------------------------------
LFSR 0: 0100110001110010011
LFSR 1: 0011111111011100111100
LFSR 2: 1101101110101100011101 1
Output (63 bits preenchidos): 0111001010010011010010011110001001000111100000100110101000100100
*** Burst de zeros detectado neste estado ***
```

```
*** Burst repetido detectado neste estado ***

Estado 64:
----------------------------------------
LFSR 0: 1001100011100100110
LFSR 1: 0111111110111001111000
LFSR 2: 1011011101011000111011 0
Output (64 bits preenchidos): 0111001010010011010010011111000100100011110000010011010100010010 0
*** Burst de zeros detectado neste estado ***
*** Burst repetido detectado neste estado ***

Propriedades de erro detectadas nos estados: [7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 3
2, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64]
----------------------------------------------------------------------------------------------------

Para k = 64 e t = 20:

Estado 0:
----------------------------------------
LFSR 0: 0111010100100100000
LFSR 1: 0110110000010000000101
LFSR 2: 0000111110111101011101
Output (0 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 1:
----------------------------------------
LFSR 0: 1110101001001000001
LFSR 1: 1101100000100000001011
LFSR 2: 0001111101111101011101 0
Output (1 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 2:
----------------------------------------
LFSR 0: 1101010010010000011
LFSR 1: 1011000001000000010110
LFSR 2: 0001111101111101011101 0
Output (2 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000000

Estado 3:
----------------------------------------
LFSR 0: 1010100100100000111
LFSR 1: 0110000010000000101101
LFSR 2: 0001111101111101011101 0
Output (3 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100

Estado 4:
----------------------------------------
LFSR 0: 0101001001000001110
LFSR 1: 0110000010000000101101
LFSR 2: 0011111011111010111010 1
Output (4 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100

Estado 5:
----------------------------------------
LFSR 0: 1010010010000011101
LFSR 1: 1100000100000001011011
LFSR 2: 0011111011111010111010 1
Output (5 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000000100

Estado 6:
----------------------------------------
LFSR 0: 0100100100000111011
LFSR 1: 1000001000000010110110
LFSR 2: 0011111011111010111010 1
Output (6 bits preenchidos): 0000000000000000000000000000000000000000000000000000000000100100

Estado 7:
----------------------------------------
LFSR 0: 1001001000001110111
LFSR 1: 0000010000000101101101
LFSR 2: 0011111011111010111010 1
Output (7 bits preenchidos): 0000000000000000000000000000000000000000000000000000000001100100

Estado 8:
----------------------------------------
LFSR 0: 0010010000011101111
LFSR 1: 0000100000001011011010
LFSR 2: 0011111011111010111010 1
Output (8 bits preenchidos): 0000000000000000000000000000000000000000000000000000000001100100

Estado 9:
----------------------------------------
LFSR 0: 0100100000111011110
LFSR 1: 0001000000010110110100
LFSR 2: 0011111011111010111010 1
Output (9 bits preenchidos): 0000000000000000000000000000000000000000000000000000000001100100

Estado 10:
----------------------------------------
LFSR 0: 1001000001110111101
LFSR 1: 0010000000101101101000
LFSR 2: 0111110111110101110101 1
Output (10 bits preenchidos): 0000000000000000000000000000000000000000000000000000001001100100

Estado 11:
----------------------------------------
LFSR 0: 1001000001110111101
LFSR 1: 0100000001011011010000
LFSR 2: 1111101111101011101011 1
Output (11 bits preenchidos): 0000000000000000000000000000000000000000000000000000001001100100

Estado 12:
```

```
----------------------------------------
LFSR 0: 0010000011101111011
LFSR 1: 1000000010110110100001
LFSR 2: 1111011111010110101110
Output (12 bits preenchidos): 000000000000000000000000000000000000000000000000000001001100100

Estado 13:
----------------------------------------
LFSR 0: 0100000111011110111
LFSR 1: 0000000101101101000011
LFSR 2: 1111011111010110101110
Output (13 bits preenchidos): 0000000000000000000000000000000000000000000000000001001001100100

Estado 14:
----------------------------------------
LFSR 0: 1000001110111101111
LFSR 1: 0000001011011010000110
LFSR 2: 1110111110101110101100
Output (14 bits preenchidos): 00000000000000000000000000000000000000000000000001001001100100

Estado 15:
----------------------------------------
LFSR 0: 0000011101111011111
LFSR 1: 0000010110110100001100
LFSR 2: 1101111101011101011101
Output (15 bits preenchidos): 000000000000000000000000000000000000000000000001001001001100100

Estado 16:
----------------------------------------
LFSR 0: 0000111011110111111
LFSR 1: 0000101101101000011000
LFSR 2: 1011111010111010111011
Output (16 bits preenchidos): 0000000000000000000000000000000000000000000001101001001100100

Estado 17:
----------------------------------------
LFSR 0: 0001110111101111111
LFSR 1: 0000101101101000011000
LFSR 2: 0111110101110101110110
Output (17 bits preenchidos): 00000000000000000000000000000000000000000000001101001001100100

Estado 18:
----------------------------------------
LFSR 0: 0001110111101111111
LFSR 1: 0001011011010000110000
LFSR 2: 1111101011101011101101
Output (18 bits preenchidos): 000000000000000000000000000000000000000000001011101001001100100

Estado 19:
----------------------------------------
LFSR 0: 0011101111011111111
LFSR 1: 0010110110100001100000
LFSR 2: 1111010111010111011010
Output (19 bits preenchidos): 0000000000000000000000000000000000000000000011011101001001100100

Estado 20:
----------------------------------------
LFSR 0: 0111011110111111111
LFSR 1: 0101101101000011000000
LFSR 2: 1110101110101110110100
Output (20 bits preenchidos): 00000000000000000000000000000000000000000000111011101001001100100

Estado 21:
----------------------------------------
LFSR 0: 1110111101111111111
LFSR 1: 0101101101000011000000
LFSR 2: 1101011101011101101001
Output (21 bits preenchidos): 000000000000000000000000000000000000000000001110111101001001100100

Estado 22:
----------------------------------------
LFSR 0: 1101111011111111110
LFSR 1: 0101101101000011000000
LFSR 2: 1010111010111001101001 0
Output (22 bits preenchidos): 000000000000000000000000000000000000000000011101101001001100100

Estado 23:
----------------------------------------
LFSR 0: 1011110111111111101
LFSR 1: 0101101101000011000000
LFSR 2: 0101110101110011010010 1
Output (23 bits preenchidos): 0000000000000000000000000000000000000000001001110110100100110010 0

Estado 24:
----------------------------------------
LFSR 0: 1011110111111111101
LFSR 1: 1011011010000110000001
LFSR 2: 1011101011100110100101 0
Output (24 bits preenchidos): 00000000000000000000000000000000000000000110011101101001001100100

Estado 25:
----------------------------------------
LFSR 0: 1011110111111111101
LFSR 1: 0110110100001100000011
LFSR 2: 0111010111001101001010 0
Output (25 bits preenchidos): 000000000000000000000000000000000000000011100111011010010011001 00

Estado 26:
----------------------------------------
LFSR 0: 0111101111111111011
LFSR 1: 0110110100001100000011
LFSR 2: 1110101110011010010 1001
```

```
Output (26 bits preenchidos): 00000000000000000000000000000000000000111100111011010010011001 00

Estado 27:
----------------------------------------
LFSR 0: 1111011111111110110
LFSR 1: 0110110100001100000011
LFSR 2: 1101011100110100101001 1
Output (27 bits preenchidos): 000000000000000000000000000000000000001111001110110100100110010 0

Estado 28:
----------------------------------------
LFSR 0: 1111011111111110110
LFSR 1: 1101101000011000000111
LFSR 2: 1010111001101001010011 0
Output (28 bits preenchidos): 0000000000000000000000000000000000000101111001110110100100110010 0

Estado 29:
----------------------------------------
LFSR 0: 1110111111111101100
LFSR 1: 1011010000110000001110
LFSR 2: 0101110011010010100110 1
Output (29 bits preenchidos): 00000000000000000000000000000000000001011110011101101001001100100

Estado 30:
----------------------------------------
LFSR 0: 1101111111111011000
LFSR 1: 0110100001100000011101
LFSR 2: 0101110011010010100110 1
Output (30 bits preenchidos): 000000000000000000000000000000000001010111100111011010010011001 00

Estado 31:
----------------------------------------
LFSR 0: 1101111111111011000
LFSR 1: 1101000011000000111011
LFSR 2: 1011100110100101001101 1
Output (31 bits preenchidos): 0000000000000000000000000000000000110101111001110110100100110010 0

Estado 32:
----------------------------------------
LFSR 0: 1101111111111011000
LFSR 1: 1010000110000001110110
LFSR 2: 0111001101001010011011 1
Output (32 bits preenchidos): 00000000000000000000000000000000001101011110011101101001001100100

Estado 33:
----------------------------------------
LFSR 0: 1011111111110110001
LFSR 1: 1010000110000001110110
LFSR 2: 1110011010010100110111 0
Output (33 bits preenchidos): 000000000000000000000000000000001011010111100111011010010011001 00

Estado 34:
----------------------------------------
LFSR 0: 1011111111110110001
LFSR 1: 0100001100000011101101
LFSR 2: 1100110100101001101110 1
Output (34 bits preenchidos): 0000000000000000000000000000000010110101111001110110100100110010 0

Estado 35:
----------------------------------------
LFSR 0: 0111111111101100011
LFSR 1: 0100001100000011101101
LFSR 2: 1001101001010011011101 1
Output (35 bits preenchidos): 00000000000000000000000000000010101101011110011101101001001100100

Estado 36:
----------------------------------------
LFSR 0: 0111111111101100011
LFSR 1: 1000011000000111011011
LFSR 2: 0011010010100110111011 0
Output (36 bits preenchidos): 000000000000000000000000000001101011010111100111011010010011001 00

Estado 37:
----------------------------------------
LFSR 0: 0111111111101100011
LFSR 1: 0000110000001110110111
LFSR 2: 0110100101001101110110 1
Output (37 bits preenchidos): 0000000000000000000000000000011010110101111001110110100100110010 0

Estado 38:
----------------------------------------
LFSR 0: 1111111111011000111
LFSR 1: 0000110000001110110111
LFSR 2: 1101001010011011101101 1
Output (38 bits preenchidos): 00000000000000000000000000001101011010111100111011010010011001 00

Estado 39:
----------------------------------------
LFSR 0: 1111111110110001110
LFSR 1: 0001100000011101101110
LFSR 2: 1101001010011011101101 1
Output (39 bits preenchidos): 000000000000000000000000000011010110101111001110110100100110010 0

Estado 40:
----------------------------------------
LFSR 0: 1111111101100011100
LFSR 1: 0011000000111011011100
LFSR 2: 1010010100110111011011 1
Output (40 bits preenchidos): 0000000000000000000000000000110101101011110011101101001001100100

Estado 41:
----------------------------------------
```

```
LFSR 0: 1111111011000111000
LFSR 1: 0110000001110110111000
LFSR 2: 1010010100110111011011 1
Output (41 bits preenchidos): 00000000000000000000000000011010110101111001110110100100110010 0

Estado 42:
----------------------------------------
LFSR 0: 1111110110001110000
LFSR 1: 0110000001110110111000
LFSR 2: 0100101001101110110111 1
Output (42 bits preenchidos): 000000000000000000000010000011010110101111001110110100100110010 0

Estado 43:
----------------------------------------
LFSR 0: 1111110110001110000
LFSR 1: 1100000011101101110001
LFSR 2: 1001010011011101101111 1
Output (43 bits preenchidos): 0000000000000000000001100000110101101011110011101101001001100100

Estado 44:
----------------------------------------
LFSR 0: 1111101100011100000
LFSR 1: 1000000111011011100010
LFSR 2: 1001010011011101101111 1
Output (44 bits preenchidos): 00000000000000000000111000001101011010111100111011010010011001 00

Estado 45:
----------------------------------------
LFSR 0: 1111101100011100000
LFSR 1: 0000001110110111000101
LFSR 2: 0010100110111011011111 0
Output (45 bits preenchidos): 000000000000000000011110000011010110101111001110110100100110010 0

Estado 46:
----------------------------------------
LFSR 0: 1111101100011100000
LFSR 1: 0000011101101110001010
LFSR 2: 0101001101110110111110 0
Output (46 bits preenchidos): 0000000000000000000111110000011010110101111001110110100100110010 0

Estado 47:
----------------------------------------
LFSR 0: 1111011000111000001
LFSR 1: 0000111011011100010100
LFSR 2: 1010011011101101111100 1
Output (47 bits preenchidos): 00000000000000000001111100000110101101011110011101101001001100100

Estado 48:
----------------------------------------
LFSR 0: 1110110001110000010
LFSR 1: 0001110110111000101000
LFSR 2: 0100110111011011111001 1
Output (48 bits preenchidos): 000000000000000010111110000011010110101111001110110100100110010 0

Estado 49:
----------------------------------------
LFSR 0: 1101100011100000100
LFSR 1: 0011101101110001010000
LFSR 2: 1001101110110111110011 0
Output (49 bits preenchidos): 0000000000000000101111100000110101101011110011101101001001100100

Estado 50:
----------------------------------------
LFSR 0: 1011000111000001000
LFSR 1: 0111011011100010100000
LFSR 2: 1001101110110111110011 0
Output (50 bits preenchidos): 00000000000000001011111000001101011010111100111011010010011001 00

Estado 51:
----------------------------------------
LFSR 0: 0110001110000010000
LFSR 1: 1110110111000101000001
LFSR 2: 0011011101101111100110 0
Output (51 bits preenchidos): 000000000000010010111110000011010110101111001110110100100110010 0

Estado 52:
----------------------------------------
LFSR 0: 1100011100000100000
LFSR 1: 1101101110001010000010
LFSR 2: 0011011101101111100110 0
Output (52 bits preenchidos): 0000000000000100101111100000110101101011110011101101001001100100

Estado 53:
----------------------------------------
LFSR 0: 1000111000001000001
LFSR 1: 1011011100010100000100
LFSR 2: 0011011101101111100110 0
Output (53 bits preenchidos): 00000000000001001011111000001101011010111100111011010010011001 00

Estado 54:
----------------------------------------
LFSR 0: 1000111000001000001
LFSR 1: 0110111000101000001001
LFSR 2: 0110111011011110011000
Output (54 bits preenchidos): 000000000010010010111110000011010110101111001110110100100110010 0

Estado 55:
----------------------------------------
LFSR 0: 0001110000010000010
LFSR 1: 1101110001010000010011
LFSR 2: 0110111011011110011000
Output (55 bits preenchidos): 0000000001100100101111100000110101101011110011101101001001100100
```

```
Estado 56:
----------------------------------------
LFSR 0: 0001110000010000010
LFSR 1: 1011100010100000100110
LFSR 2: 1101110110111100110001
Output (56 bits preenchidos): 00000000011001001011110000011010110101111001110110100100110010

Estado 57:
----------------------------------------
LFSR 0: 0011100000100000101
LFSR 1: 0111000101000001001101
LFSR 2: 1101110110111100110001
Output (57 bits preenchidos): 000000010110010010111110000011010110101111001110110100100110010

Estado 58:
----------------------------------------
LFSR 0: 0111000001000001011
LFSR 1: 0111000101000001001101
LFSR 2: 1011101101111001100010
Output (58 bits preenchidos): 0000001101100100101111100000110101101011110011101101001001100100

Estado 59:
----------------------------------------
LFSR 0: 1110000010000010110
LFSR 1: 1110001010000010011011
LFSR 2: 1011101101111001100010
Output (59 bits preenchidos): 00000111011001001011110000011010110101111001110110100100110010 0

Estado 60:
----------------------------------------
LFSR 0: 1100000100000101101
LFSR 1: 1100010100000100110110
LFSR 2: 1011101101111001100010
Output (60 bits preenchidos): 000011110110010010111110000011010110101111001110110100100110010 0

Estado 61:
----------------------------------------
LFSR 0: 1000001000001011010
LFSR 1: 1000101000001001101100
LFSR 2: 1011101101111001100010
Output (61 bits preenchidos): 0001111101100100101111100000110101101011110011101101001001100100

Estado 62:
----------------------------------------
LFSR 0: 0000010000010110101
LFSR 1: 0001010000010011011001
LFSR 2: 1011101101111001100010
Output (62 bits preenchidos): 00111111011001001011110000011010110101111001110110100100110010 0

Estado 63:
----------------------------------------
LFSR 0: 0000010000010110101
LFSR 1: 0010100000100110110010
LFSR 2: 0111011011110011000100
Output (63 bits preenchidos): 00111111011001001011110000011010110101111001110110100100110010 0

Estado 64:
----------------------------------------
LFSR 0: 0000100000101101011
LFSR 1: 0101000001001101100100
LFSR 2: 0111011011110011000100
Output (64 bits preenchidos): 00111111011001001011110000011010110101111001110110100100110010 0

> Nenhuma propriedade de erro detectada para burst de tamanho 20.
```

Influência do parâmetro k (número de iterações)

- Se o número de passos k é pequeno, o sistema tem menos oportunidades de gerar um burst de zeros ou de repetir um padrão de tamanho t. Isso reduz a probabilidade de ocorrência de ambas as propriedades de erro.
- À medida que aumentamos k, o sistema tem mais iterações e portanto mais sequências possíveis de saída. Isto aumenta a probabilidade de ser detectado um burst de zeros ou um burst repetido no limite de passos definido.

Influência do parâmetro t (tamanho do burst)

- Se t é pequeno, o burst ocorre mais facilmente, uma vez que a repetição de um padrão curto de bits é mais provável do que um padrão comprido.
- À medida que aumentamos t, a ocorrência de um mesmo burst de zeros torna-se menos provável, assim como a repetição de um burst, uma vez que existem mais combinações possíveis para t bits.

Conclui-se que o aumento de k torna as propriedades de erro mais prováveis, enquanto que o aumento de t torna as propriedades de erro menos prováveis.